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EES Hardware Integration Guide

Embedded Ethernet Switch Product Family

EES20 and EES25

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Contents

Safety instructions

This documentation contains instructions which must be observed to ensure your own personal safety and to avoid damage to devices and machinery.

- **Certified usage**

  The device may only be employed for the purposes described in the catalog and technical description, and only in conjunction with external devices and components recommended or approved by the manufacturer. The product can only be operated correctly and safely if it is transported, stored, installed and assembled properly and correctly. Furthermore, it must be operated and serviced carefully.

- **Qualification requirements for personnel**

  Qualified personnel as understood in this manual and the warning signs are persons who are familiar with the setup, assembly, startup, and operation of this product and are appropriately qualified for their job. This includes, for example, those persons who have been:

  - ► trained or directed or authorized to switch on and off, to ground and to label power circuits and devices or systems in accordance with current safety engineering standards;
  - ► trained or directed in the care and use of appropriate safety equipment in accordance with the current standards of safety engineering;
  - ► trained in providing first aid.

- **National and international safety regulations**

  - ☐ Make sure that the electrical installation meets local or nationally applicable safety regulations.

- **Note on the CE marking**

  The EES is not intended for end users in accordance with item 2(1)b) of the EMC Directive 2004/108/EG. See also chapter 1.2 in “Guide for the EMC Directive 2004/108/EC (21st May 2007)”. The manufacturer or distributor of the end device in which the EES was installed, is responsible for adhering to the applicable EU directives, as well as the CE marking.

  The EES adheres to the EMC standards as listed in section 5.1 of this document.

The EMC tests were performed in combination with the Evaluation Board.

- **Maintenance**

  - ☐ When designing this device, Hirschmann was largely able to forego using wear parts. The parts subject to wear are dimensioned to last longer than the lifetime of the product when it is operated normally.
  - ☐ Relays are subject to natural wear. This wear depends on the frequency of the switching operations. Check the resistance of the closed relay contacts and the switching function periodically according to the frequency of the switching operations.
  - ☐ Hirschmann continually works on improving and developing their software. You should regularly check whether there is a new version of the software that provides you with additional benefits. You will find software information and downloads on the product pages of the Hirschmann website.

- **ESD guidelines**

  The media modules contain components highly sensitive to electrostatic fields. These components can be easily destroyed or have their lives shortened by an electrical field or by a discharge caused by touching the contacts. You can find more information about devices vulnerable to electrostatic fields in IEC/TR 61340-5-2 (2007-08)

- **Recycling note**

  After usage, this product must be disposed of properly as electronic waste, in accordance with the current disposal regulations of your county, state and country.

About this Guide

This document provides technical specifications for the Embedded Ethernet Switch (EES) development board. It also illustrates hardware integration guidelines for a Hirschmann Embedded Ethernet Switch (EES) module. It describes the board level interfaces as well as the key operation parameters. Additionally, it provides the necessary information for a developer to validate their application design using the EES development board.

The information in this publication merely contain general descriptions or performance factors which, when applied in an actual situation, do not always correspond with the described form and may be amended by way of the further development of products. The desired performance factors shall only be deemed binding if these are expressly agreed on conclusion of the contract. Please note that some characteristics of the recommended accessory parts may differ from the appropriate product. This might limit the possible operating conditions for the entire system.

References

On the EES Development Kit CD you can find additional documents for the development board. It is recommended to use these documents when developing your application.

- ► EES development board schematics in .PDF format
- ► EES development board schematics in ORCAD format
- ► EES development board Gerber files
- ► EES development board PCB layout files
- ► VHDL code of EES development board CPLD

Legend

The symbols used in this manual have the following meanings:

►	Listing
□	Work step
■	Subheading

Revision History

Version	Date	Page	Description
1.0	04/2012		New Create Preliminary
1.1	08/2012	26	Added - Alternative SPI implementation and assembly option
1.2	01/2013	20, 21, 22 and 24 31, 32, 33 34 35	Updated the applications and assembly notes for Tx- and Fx-Modes Added and updated - Switching parameter Added - Electrical Specification: Reduction of power Consumption Changed - Electrical Specification: Fx- Mode: Input sensitivity to $V_{I\ DIFF\ min.}$ = 500mV
1.3	03/2013	22, 26	Application and assembly information changed
1.4	03/2013	28 29,30	Added - Host device connection over an Ethernet Interface Added - Capacitive and Magnetic Coupling
1.5	06/2013	16 20 41	Added - Heat Spreader - Note: Redundancy protocols - MTBF Value

1 Development Board Interfaces

1.1 Overview

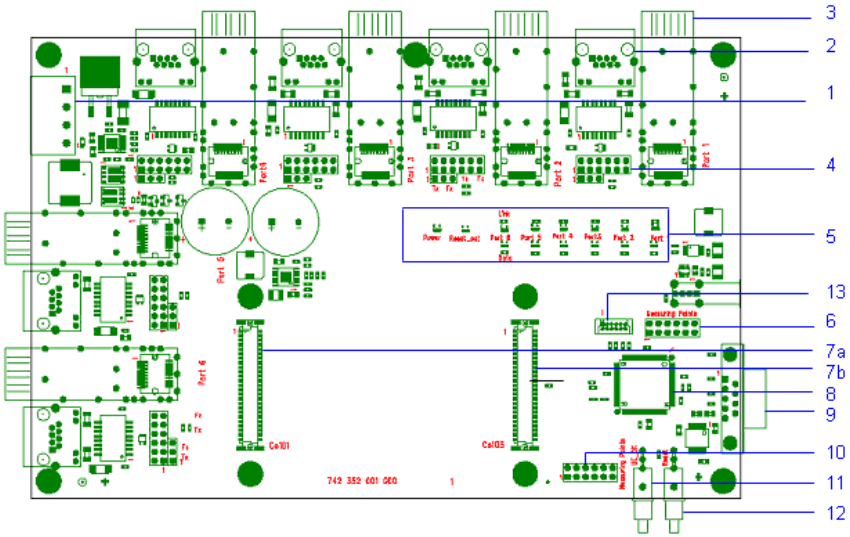


Figure 1-1: Components of the PCB Assembly

The hardware development board offers:

(1) DC Jack for 24 VDC external power supply

(2) 6 * Magnetics + RJ45 connector for 10/100Base-TX.

(3) 6 * SFP cages for 100Base-FX transceivers.

(4) Jumper for setting hardware mode to 10/100Base-TX or 100Base-FX

(5) LEDs for status information per port of link and data activity as well for device status

(6) 12-pin header with signals as measuring points (CO303)

(7a) 50-pin, dual-row vertical female EES connectors (CO101)

(7b) 50-pin, dual-row vertical female EES connectors (CO103)

(8) CPLD for control signals

(9) RS-232 connector (SubD-9) for serial communication

(10) 12-pin header with signals as measuring points (CO102)

(11) Push button: “UE_ok”

(12) Push button: “RESET”

(13) PLD JTAG connector (CO301)

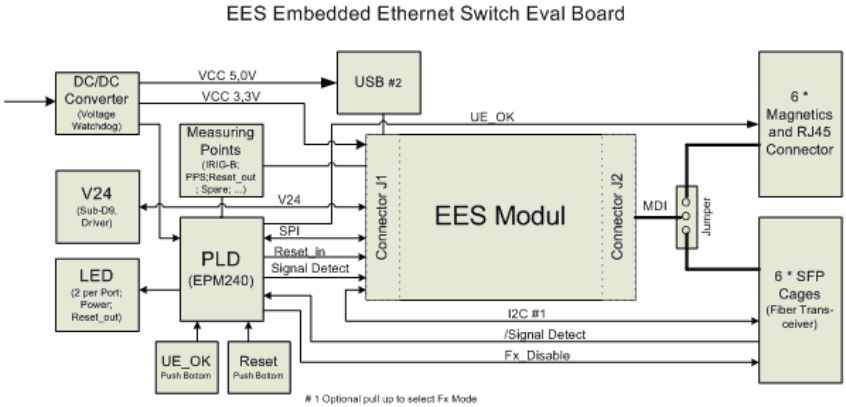


Figure 1-2: Block diagram development Board

1.2 Power supply

Connect the DC jack on the baseboard to a 24 VDC power supply. Connect pins (1, 4) of the jack to +UE and the center pins (2, 3) of the jack to GND.

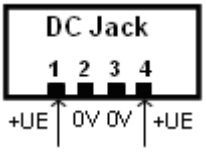


Figure 1-3: DC jack Connection

1.3 Twisted Pair Ethernet Interface

The 10/100 Mbit/s Ethernet ports (IEEE 802.3 10/100 Base-TX) use RJ45 sockets, and support:

- ► Auto negotiation
- ► Auto polarity
- ► Auto crossing (if auto negotiation is activated)
- ► 100 Mbit/s half-duplex mode, 100 Mbit/s full duplex mode
- ► 10 Mbit/s half-duplex mode, 10 Mbit/s full duplex mode

Default configuration: auto negotiation enabled.

Note: EES25 Ports 1 and 2 support only 100Base-TX full duplex

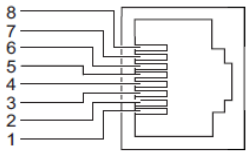
Figure	Pin	Function	
	1	RD+	Receive Data +
	2	RD-	Receive Data -
	3	TD+	Transmit Data +
	6	TD-	Transmit Data -
	4,5,7,8	Not used	

Figure 1-4: RJ45 Ethernet socket

1.4 Fiber optic Ethernet Interface

The Development Board provides SFP cages for optical Fast Ethernet (100Base-FX) SFP transceivers. Refer to the “Small Form-Factor Pluggable (SFP) Multi Sourcing Agreement” for more details on the 100Base-FX module.

1.5 Jumper Setting Ethernet Ports

Each port can operate in either 10/100Base-TX (using RJ45 connectors) or 100Base-FX mode (using the SFP cage). The device requires you to physically configure each port using five jumpers. By default each port is configured for 10/100Base-TX operation. To enable use of 100Base-FX simply remove the jumpers and place them in position as showed in figure 1-6.

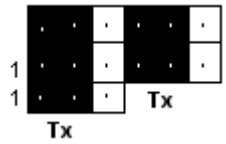


Figure 1-5: Copper communication interface enabled

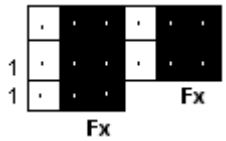


Figure 1-6 Fiber Optic communication interface enabled

Note: See chapter 3.4 for more information about setting the ports to TX or FX mode.

Note: Port mode changes are activated after resetting the device.

1.6 LED Status Indication

Link status (green LED) Port [6…1]	
Off	No valid connection.
Green	Valid connection.
Data (yellow LED) Port [6…1]	
Off	No data traffic
Yellow	Data traffic
Power (green LED)	
Off	No valid supply voltage
Green	Supply voltage available
Reset_out (green LED)	
Off	System not ready
Green	System running

Table 1-1: LED status indication

1.7 Measuring Points Connectors

The 12-pin, dual-row connectors on the baseboard give access to several EES signals. The signals are LVTTL level. The “Spare” pins (1-11), on connector CO303, are reserved for future use.

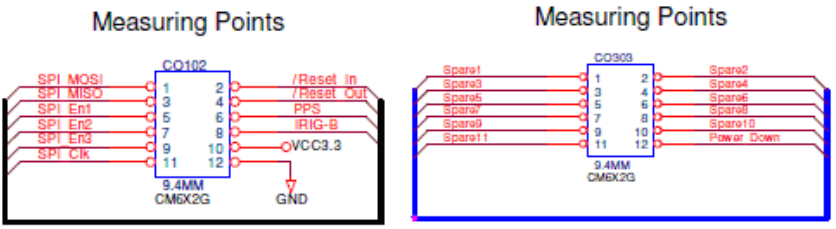


Figure 1-7: EES baseboard schematic (part Measuring points)

1.8 EES Socket (CO101/ CO103)

The 50-pin, dual-row, sockets are used to mount the EES20/25 module. For more details see chapter 2.

1.9 JTAG Connection (CPLD)

The CPLD (Altera EPM240) can be programmed via the CO301 connector.

Pin #	Signal	Pin #	Signal
1	VCC3.3	2	RTCK
3	TCK	4	TMS
5	n.c.	6	TDI
7	TDO	8	GND
9	n.c.	10	n.c.
11	n.c.	12	n.c.

Table 1-2: Pin assignment CO301

1.10 Sub D9 Socket RS232

A serial data RS232 (V24_TxD/RxD) connection is available on the baseboard to provide access to the EES. This enables you to set up a connection to the Command Line Interface (CLI) and system monitor. For more information on the CLI functionality, refer to the Command Line Interface (EES) Reference Manual.

The serial interface uses RS232 (V.24) without a hardware handshake. A SubD9 connector is mounted on the baseboard for this purpose.

RS232 socket pin description (SubD9 female):

- Pin 2 -> RxD (Data from the development board to the host)
- Pin 3 -> TxD (Data from host to development board)
- Pin 5 -> GND

Configure your terminal emulator (for example, Hyperterm, TeraTerm, PUTTY) with the following settings to issue CLI commands to the EES through the RS232 connection:

Terminal Settings	
Speed	9,600 Baud
Data	8 bit
Stop bit	1 bit
Hand shake	off
Parity	none

Table 1-3: Parameters

1.11 Push Buttons

The following push buttons are available on the EES:

- Push button “RESET“: resets the EES module
- Push button “UE_ok”: this button is for test purposes only, do not use.

2 EES Socket

2.1 Mechanics

The interconnectors on the EES20/25 development board are manufactured by ERNI (www.erni.de) part number 154807 (a stacking height of 8.0–9.5mm is obtained) as illustrated below:

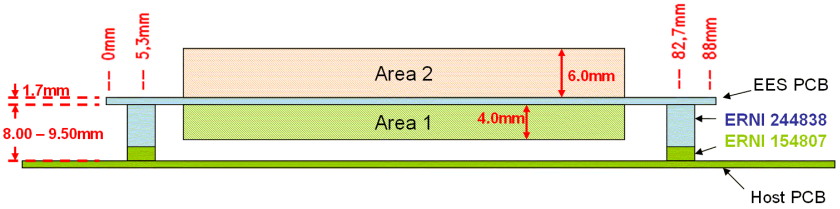


Figure 2-1: EES Board space

Alternatively, interconnector type 124045 from ERNI can be used for stacking heights of 10.8-12.3mm.

Note: the mechanical restrictions shown in figure 2-1 above. Due to the clearance height no additional external parts are allowed in areas 1 and 2.

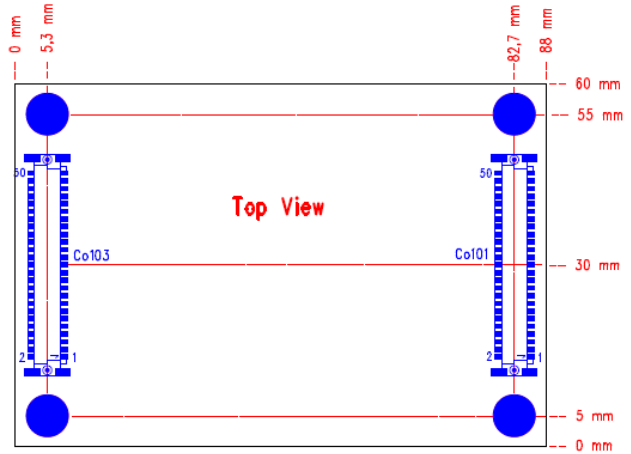


Figure 2-2: Top view EES Board

2.1.1 EES-Module with Heat Spreader

The figure below shows the position of the holes for the screws of the cooling block and the total height of the module. For details about the Heat dissipation parameters see:
“IS_OperatingTemperature_EES2025_01_0113_en.pdf”

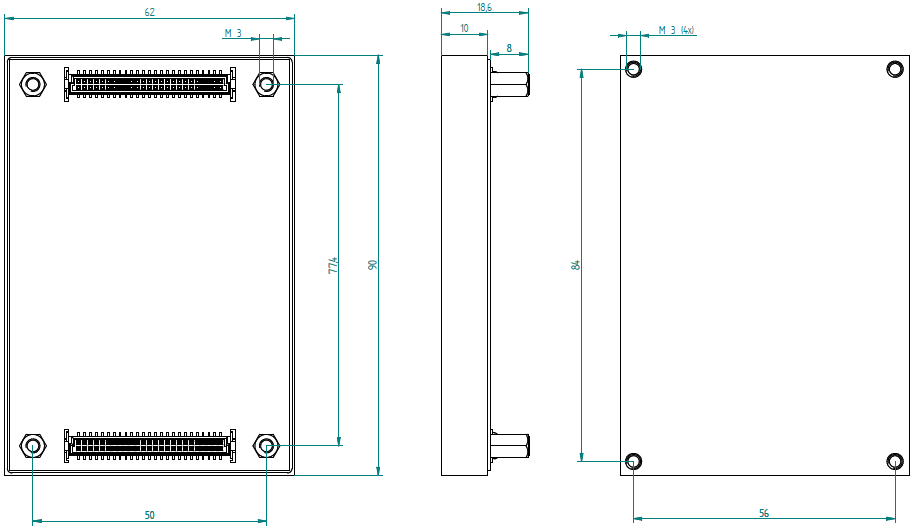


Figure 2-3: Top view EES Module including cooling block

2.2 PIN Assignment

Table 2-1 and Table 2-2 describe the pin out and signals names of the interconnectors mounted on the baseboard.

CO103				CO101			
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	GND	1	GND	2	GND
3	I2C_Clk_1	4	I2C_Data_1	3	TXP1	4	TXN1
5	I2C_Data_2	6	I2C_Clk_2	5	VCC	6	VCC
7	I2C_Clk_3	8	I2C_Data_3	7	RXP1	8	RXN1
9	I2C_Data_4	10	I2C_Clk_4	9	GND	10	GND
11	I2C_Clk_5	12	I2C_Data_5	11	TXP2	12	TXN2
13	I2C_Data_6	14	I2C_Clk_6	13	Vmag_P345	14	Vmag_P126

15	GND	16	GND	15	RXP2	16	RXN2
17	LOS_1	18	LOS_2	17	GND	18	GND
19	LOS_3	20	LOS_4	19	TXP3	20	TXN3
21	LOS_5	22	LOS_6	21	VCC	22	UeOK
23	GND	24	GND	23	RXP3	24	RXN3
25	/Reset_out	26	/Reset_in	25	GND	26	GND
27	GND	28	GND	27	TXP4	28	TXN4
29	V24_TxD	30	V24_RxD	29	VCC	30	VCC
31	V24_CTS	32	V24_RTS	31	RXP4	32	RXN4
33	GND	34	GND	33	GND	34	GND
35	SPI_Clk	36	SPI_MISO	35	TXP5	36	TXN5
37	SPI_En1	38	SPI_MOSI	37	Vmag_P345	38	Vmag_P126
39	SPI_En2	40	NC	39	RXP5	40	RXN5
41	GND	42	GND	41	GND	42	GND
43	IRIG-B (*)	44	PPS (*)	43	TXP6	44	TXN6
45	NC	46	NC	45	VCC	46	VCC
47	NC	48	NC	47	RXP6	48	RXN6
49	GND	50	GND	49	GND	50	GND

(*) EES25 only, for EES20 those pins are not connected

Table 2-1: Pin assignment of the interface connectors (CO103, CO101)

2.3 PIN Description

Signal Name	Type (EES)	Description
RXPx / RXNx	I [0] (analog)	Receive Input (negative), Receive Input (positive) Differential data from the media is received on the RXP/RXN signal pair. For 10/100Base-TX operation RXP/RXN are connected directly to the receiver magnet. For 100Base-FX RXP/RXN pair is connected to the optical receiver's outputs. All unused RXP/RXN pins shall be left unconnected. If auto MDI crossover is active, RXP/RXN pins will be changed to outputs.

Signal Name	Type (EES)	Description
TXPx / TXNx	O [I] (analog)	Transmit output (negative), Transmit output (positive) Differential data is transmitted to the media on the TXP/TXN signal pair. For 10/100Base-TX operation TXP/TXN are connected directly to the transmitter magnet. For 100Base-FX TXP/TXN pair is connected to the optical transmitter inputs. All unused TXP/TXN pins shall be left unconnected. If auto MDI crossover is active, TXP/TXN pins will be changed to inputs.
I2C_Clk_x	I/O (LVTTL)	I2C bus clock output and bus data, for ports 1…6. For each Ethernet port there is one I2C bus to connect to a SFP transceiver (only required in 100Base-FX mode if a SFP transceiver is used). Additionally, I2C_Clk_x pins can be used to pre-set the port mode during start-up. If the pin is high level during start-up, the port will be set to fiber mode (100Base-FX), while a low level will set the port to copper mode (10/100Base-TX).
I2C_Data_x	I/O (LVTTL)	
LOS_x	I (LVTTL)	“Loss_of_Signal” input. This signal indicates that a fiber optic receiver has no valid input signal. (for 100Base-FX mode only, it can be directly connected to SFP transceivers LOS signal. When using a 1*9 transceiver this signal has to be connected to the SD (signal detect) output with an inverter / level shifter)
SPI_Clk	O (LVTTL)	SPI interface providing status information from the module to the host system. EES acts as a SPI master.
SPI_MISO	I (LVTTL)	
SPI_MOSI	O (LVTTL)	
SPI_En1	O (LVTTL)	
SPI_En2	O (LVTTL)	

Signal Name	Type (EES)	Description
V24_TxD	O (LVTTL)	V.24 (RS-232) interface for configuration access to the embedded microcontroller.
V24_RxD	I (LVTTL)	
V24_CTS	I (LVTTL)	
V24_RTS	O (LVTTL)	
IRIG-B	O (LVTTL)	EES25: This pin provides IRIG-B timing information data EES20: NC
PPS	O (LVTTL)	EES25: This pin provides a pulse-per-second timing information signal EES20: NC
/Reset_in	I (LVTTL)	Reset input, active low
/Reset_out	O (LVTTL)	This pin indicates to the host that a reset of the module is in progress. Active low (The system is running when this pin goes high).
UeOK	I (LVTTL)	A high signal indicates that the Main Power Supply is OK. If UeOk signal is not used, this pin must be connected to VCC.
Vmag_P126	Power (Output)	Those pins provide DC voltage for the magnetic (only in 10/100Base-TX mode). Vmag_P126 to be used for Ports 1, 2 and 6, Vmag_P345 to be used for Ports 3, 4 and 5.
Vmag_P345	Power (Output)	
VCC	Power	Power Supply for the EES module (3,3V)
GND	Power	Power Supply- Ground
NC		These pins must be left unconnected

Table 2-2: Pin Descriptions

3 Application Guide Line

This chapter provides recommendations for implementation of the Ethernet and SPI interfaces.

Note: The EES20/25 Module redundancy protocols (RSTP and MRP) are Software based and run on 10/100BaseTx, 100BaseFx Fast Ethernet ports, Port [1..6].
The EES25 Module redundancy protocols (HSR, PRP and Fast-MRP) are Hardware based and run on Ethernet ports (port # 1, port # 2) exclusively.

3.1 Ethernet interface for 10/100Base-TX connection

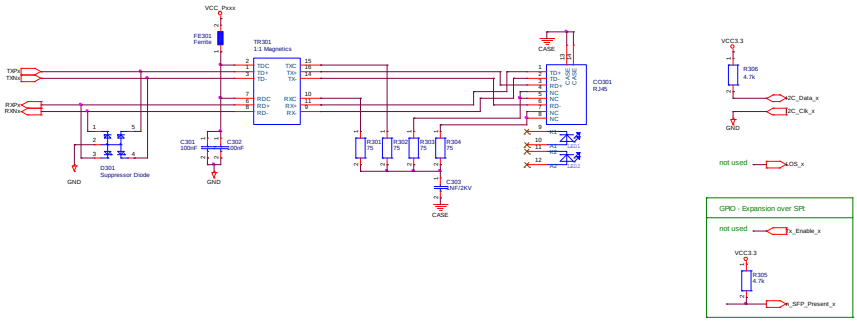


Figure 3-1: 10/100Base-TX interface recommendation

Signal Description: VCC_Pxxx		
	EES25 (FPGA Version)	EES20 (CPLD Version)
Port-1	Vmag_P126	Vmag_P126
Port-2	Vmag_P126	Vmag_P126
Port-3	Vmag_P345	Vmag_P345
Port-4	Vmag_P345	Vmag_P345
Port-5	Vmag_P345	Vmag_P345
Port-6	Vmag_P126 (VCC3.3)	VCC3.3

Signal Description:	
GND	Signal - Ground
CASE	Chassis - Ground

Table 3-1: 10/100Base-TX center tap voltage

For operational reasons the ports require different supply voltages for the center taps of the magnetic poles. See table 3-1 for details.

For EES20 Port-6 only:
It is recommended to turn on the VCC3.3 after Vmag_P126 (2,5V).

3.2 Ethernet interface for 100Base-FX

3.2.1 Interface connection (SFP Transceiver)

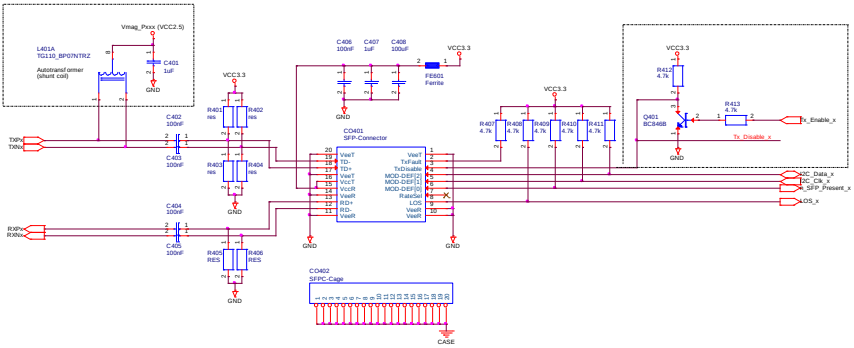


Figure 3-2: 100Base-FX (SFP) interface recommandation

Components: C401 - 1µF L401 - TG110-BP07NTRL (Halo) or TG110-BP01NURL (Halo) or HX2358NL or HX2359NL (Pulse)		
	EES25 (FPGA Version)	EES20 (CPLD Version)
Port-1	not use	assemble
Port-2	not use	assemble
Port-3	assemble	assemble
Port-4	assemble	assemble
Port-5	assemble	assemble
Port-6	not use	not use

Tx_Enable / Tx_Disable - Option:	
when used with Shift Register	when used with Prog. Logic
1) connect Tx_Enable_x 2) External Inv. required (assemble - R412, R413, Q401)	1) connect Tx_Disable_x 2) External Inv. not required (not used - R412, R413, Q401)
x => Port 1 - Port 6	

Signal Description:	
GND	Signal - Ground
CASE	Chassis - Ground

Table 3-2: 100Base-FX (SFP) schematic information

3.2.2 Interface connection (1*9 Transceiver)

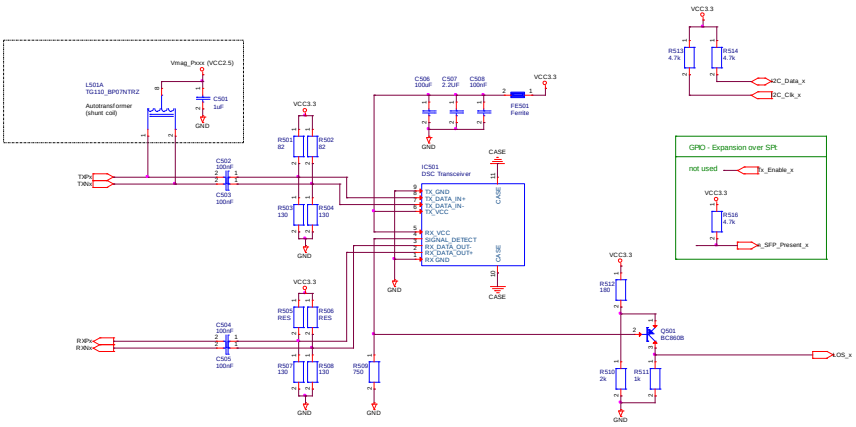


*Figure 3-3: 100Base-FX (1*9 transceiver) interface recommendation*

Components: C501 - 1µF L501 - TG110-BP07NTRL (Halo) or TG110-BP01NURL (Halo) or HX2358NL or HX2359NL (Pulse)		
	EES25 (FPGA Version)	EES20 (CPLD Version)
Port-1	not use	assemble
Port-2	not use	assemble
Port-3	assemble	assemble
Port-4	assemble	assemble
Port-5	assemble	assemble
Port-6	not use	not use

Signal Description:	
GND	Signal - Ground
CASE	Chassis - Ground

*Table 3-3: 100Base-FX (1*9 transceiver) schematic information*

For operational reasons the ports require different circuits. See table 3-3 for details.

3.3 SPI Interface connection

EES provides a SPI interface (acts as SPI master) for status indication.

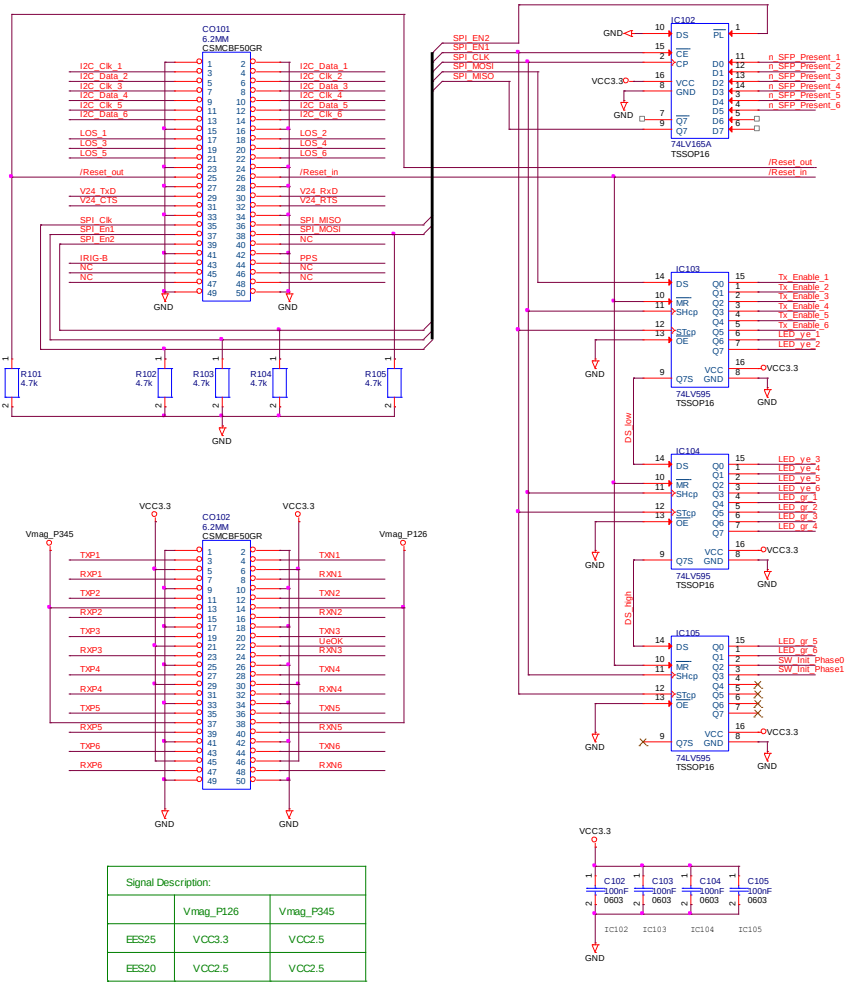
The EES development board communicates with the on-board CPLD via a SPI interface. The CPLD serializes and de-serializes the SPI data stream and provides the signals to I/O pins.

Pin	Direction *	Description
SPI_En1	Serial Control Output	Control signals, Storage Register
SPI_En2	Serial Control Output	Control signals, Parallel load
SPI_Clk	Serial Data clock	The clock signal produced from the master device to synchronize the data transfer
SPI_MOSI	Serial Data Output	SPI data, **m**aster **o**ut/**s**lave **i**n
SPI_MISO	Serial Data Input	SPI data, **m**aster **i**n/**s**lave **o**ut

* With respect to the EES

Table 3-4: SPI connector pin assignment

The SPI-pin out definitions are described in Table 3-4. In the target application, the CPLD can be replaced with standard logic shift registers, for example, 74HC595 or 74HC165 (see figure 3-4).



Signal Description:		
	Vmag_P126	Vmag_P345
EES25	VCC3.3	VCC2.5
EES20	VCC2.5	VCC2.5

Figure 3-4: SPI implementation example

3.3.1 SPI Protocol Timing

Figure 3-5 illustrates every timing parameter in the SPI Protocol. These timing parameters are a result of the EES internal operation and both constrain host behavior and characterize EES operation. Note that Figure 3-5 is not drawn to scale, but is instead drawn only to illustrate where the parameters are measured. The EES is the master and sends data on SPI_MOSI and receives data on SPI_MISO.

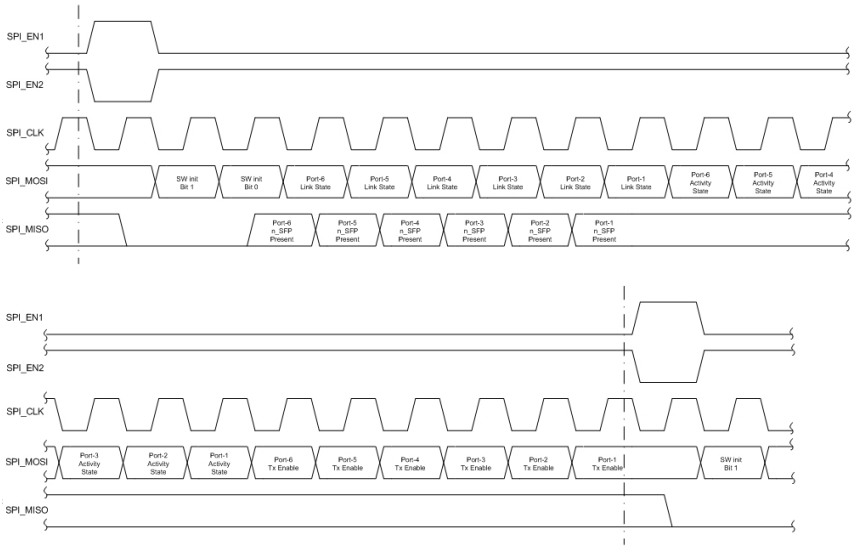


Figure 3-5: SPI Timing Diagram

Reading signals from the EES is similar to writing to it. The SPI_En read/write command is sent first, followed by send and receives information in 20 bit patterns. The EES transmits link and data activity status information for every port. It transmits general status information to the host system on SPI_MOSI and also reads status information from the host system on SPI_MISO, providing a SFP transceiver is installed.

Bit	Name	Description
19…18	Firmware_Init_Status	Status of firmware during boot phase, tbd
17…12	Link_State[6…1]	Link status for ports 6 … port 1, high = link, low = no link
11…06	Activity_State[6…1]	Port activity for ports 6 … port 1, high = activity, low = no activity
05…00	Transceiver_Enable[6…1]	Enable signal for optical transceivers. Low=transceiver disabled, high = transceiver enabled

Table 3-5: SPI transmitted information (from EES to host system)

This information can be read from the host CPU or interpreted from dedicated hardware on the host system, for example, drive port status LEDs.

Bit	Name	Description
19…18	not used	-
17…12	N_SFP_present[6..1]	Low = SFP module is present High = SFP module is not present
11…06	not used	-
05…00	not used	-

Table 3-6: SPI received information (from host system to EES)

If the target application work without SPI – GPIO expansion then it is necessary to connect the SPI_MISO signal as follows…

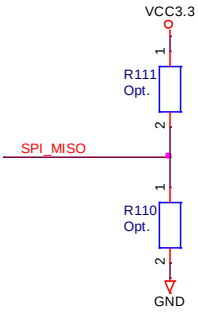


Figure 3-6: Alternative SPI implementation example

Configuration without SPI - GPIO Expansion (This applies to all Ports)		
Port 1..6	Tx - Mode (Copper) Fx - Mode (DSC/DST) (without I2C Interface)	Fx - Mode (SFP) (with I2C Interface)
R111 R110	4.7k not used	not used 4.7k

Table 3-7: Assembly information for alternative example

3.4 I2C Interface connection

For each Ethernet port there is one I2C bus connected to a SFP transceiver. This connection is only required for the 100Base-FX mode in which a SFP transceiver is used. This interface can be used to read transceiver status information, such as transceiver type, temperature, optical receive power and other information provided by the selected SFP transceiver.

In addition, the I2C_Clk_x pins are used to pre-set the port mode during start-up. If a high level is detected on the pin during start-up, the port will be set to fiber mode (100Base-FX), while the detection of a low level will set the port to copper mode (10/100Base-TX). To set the I2C_Clk_x line to a high level, connect a 4.7KOhm pull-up resistor to the VCC3.3 supply. Connect the I2C_Clk_x pin directly to GND for TX mode.

3.5 Time Synchronization (EES25 only)

The EES25 provides two timing outputs, a PPS and an IRIG-B, which are connected to the internal PTP slave. These outputs can be used to provide precise synchronization to the host system. The system clock is further distributed via IEEE 1588.

Note: The master is always the device (EES) that drives the Clk clock line.

3.5.1 PPS

The EES25 provides a PPS (pulse per second) output signal that is connected to the PTP slave unit. The leading edge of PPS signal indicates the beginning of each second. The PPS signal has a 20% duty cycle, consisting of a 200ms high level followed by a 800ms low level. The output is a LVTTL signal.

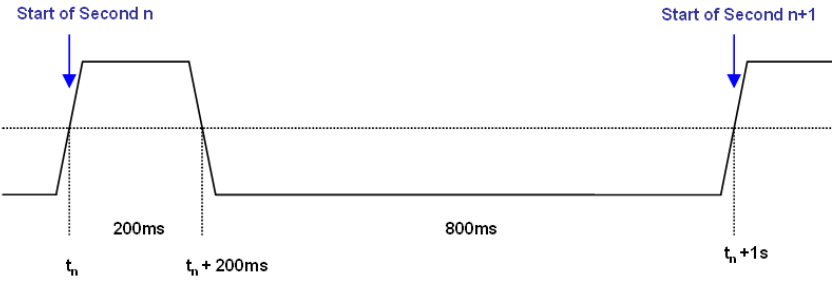


Figure 3-7: PPS Output Timing Diagram

3.5.2 IRIG-B

The EES provides a standard IRIG-B output signal with LVTTL. This signal is controlled by the PTP slave clock. Un-modulated formats B000, B001, B002, B003, B004, B005, B006 and B007 are supported.

3.6 Host Device connection over an Ethernet Interface

This chapter describes a connecting of the EES module to a host device. The application is approved only for the port 6.

Devices for a galvanic separation are not present on the EES module itself. Appropriate isolation can be achieved by using an external 1:1-Ethernet transformer.

If no electrical isolation is required, the module can also be connected directly to another Ethernet PHY device. In this case, capacitive coupling can be applied.

3.6.1 Capacitive Coupling – 100Base-FX

The Ethernet signals TXP6/TXN6, RXP6/RXN6 shall be coupled directly with a capacitor (100 nF). The port-6 shall be operated in FX-Mode (see figure 3-8).

On the host device side, the circuit is dependent of the used PHY component. Please refer to the data sheet of the appropriate PHY vendor.

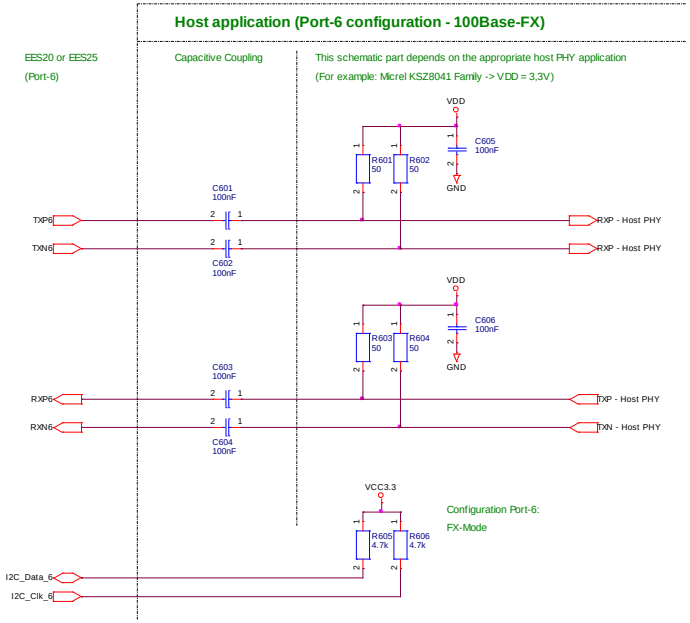


Figure 3-8: Capacitive Coupling - Circuit Diagram

3.6.2 Magnetics Coupling – 10/100Base-TX

The Ethernet signals TXP6/TXN6, RXP6/RXN6 shall be coupled with a magnetic transformer. The port-6 shall be operated in TX-Mode (see figure 3-9).

On the host device side, the circuit is dependent of the used PHY component. Please refer to the data sheet of the appropriate PHY vendor.

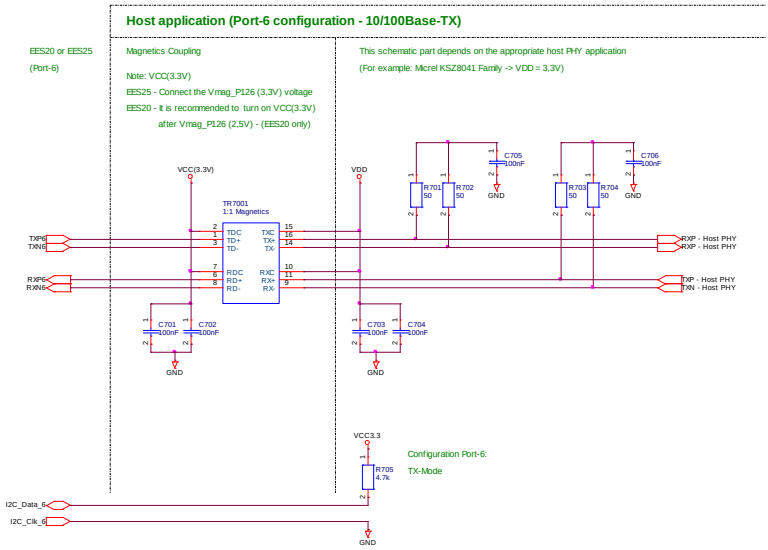


Figure 3-9: Magnetics Coupling - Circuit Diagram

4 Technical Data

Parameter		Min.	typ.	max.	Dim.
Switch type (Standard Ports)			Store-and-Forward		
Latency (end receive – begin transmit)					
10Mbit; 64 ... 1518 Byte Paketlänge		5,0	7,8	10,0	µs
100Mbit; 64 ... 1518 Byte Paketlänge		6,0	8,0	11,0	µs
Switch type (EES25 – (Port-1, Port-2) ⇔ all other ports)			Store-and-Forward		
Latency (end receive – begin transmit)					
100Mbit; 64 Byte Paketlänge	HSR or PRP on		15,0		µs
	HSR and PRP off		8,0		µs
100Mbit; 1518 Byte Paketlänge	HSR or PRP on		130,6		µs
	HSR and PRP off		8,0		µs
Switch type (HSR on) (EES25 – (Port-1 ⇔ Port-2))			cut-through		
Latency (end receive – end transmit)					

100Mbit; 64 ... 1518 Byte Paketlänge		8,8		µs
Switch type (PRP on) (EES25 - Port-1 ⇔ Port-2)		no-forwarding		
Address table			2k	addresses
Packet buffer				
all ports (pages with 256 Byte)			64	kByte
Packet memory receive				
per port (64 Byte Paket)			59	packets
per port (1518 Byte Packet)			11	packets
length of transmit queue per port				
Low/ high priority queue (64 Byte Packet)			18	packets
Low/ high priority queue (1518 Byte Packet)			3	packets
Priority				
number of priority queues	4	4	4	
strict priority		yes		
priority-tag to lowest priority queue		1; 2 w/o tagging		
priority-tag to low priority queue		3,0		
priority-tag to high priority queue		4,5		
priority-tag to highest priority queue		6,7		

Switch fabric capacity				600	MBit/s
Packet throughput per port (Standard)				**full wire speed**	
100Mbit; 64 Byte Paketlänge		-	-	148.809	Packets/s
100Mbit; 1518 Byte Paketlänge		-	-	8.127	Packets/s
Packet throughput per port (HSR or PRP on)					
100Mbit; 64 Byte	HSR		63.243 (42,5%)	138.888 (93%)	Packets/s
	PRP	-	tbd (< 46,5%)	138.888 (93%)	Packets/s
100Mbit; 1518 Byte	HSR		3.957 (48,7%)	8.095 (99%)	Packets/s
	PRP	- -	tbd (< 49,5%)	8.095 (99%)	Packets/s

Table 4-1: Switch parameter

Symbol	Description	min.	typ.	Max.	Units
VCC24	Supply voltage Development Board (DC)	+18	+24	+32	V
VCC3.3	Supply voltage EES	3,168 (-4%)	+3,3	+3,465 (+5%)	V
VCC3.3	Maximum Ripple EES (AC)			+/- 50pp	mV

Symbol	Description	min.	typ.	Max.	Units
P_{IN} (VCC3.3)	Power Consumption EES25 (all ports activ) Tx-Mode/ Fx-Mode		4,6 (15,7)	5,1 (17,4)	W (BTU/h)
$P_{IN\ (VCC24)}$	Power Consumption Eval. Board + EES25 (all ports activ) Tx-Mode Fx-Mode		6,6 (22,6) 11,8 (40,4)	7,4 (25,3) 12,4 (42,4)	W (BTU/h) W (BTU/h)
P_{IN} (VCC3.3)	Power Consumption EES20 (all ports activ) Tx-Mode/ Fx-Mode		2,9 (9,9)	3,3 (11,3)	W (BTU/h)
$P_{IN\ (VCC24)}$	Power Consumption Eval. Board + EES20 (all ports activ) Tx-Mode Fx-Mode		4,7 (16,1) 9,6 (32,8)	5,4 (18,5) 10,4 (35,6)	W (BTU/h) W (BTU/h)
$P_{Economy}$ (VCC3.3)	Reduction of power Consumption per disabled port #1		- 0,12		W
V_{IH}	High-level input voltage	2,0		VCC3.3	V
V_{IL}	Low-level input voltage	0		0,8	V
V_{OH}	High-level Output voltage (I_{OH} = 4mA)	2,4			V
V_{OL}	Low-level Output voltage (I_{OL} = - 4mA)			0,45	V

Table 4-2: Electrical Specification

Note: The items marked with "#1" : The power consumption (VCC3.3) is reduced typically by 0,12W for each disabled port. This is not dependent on the EES Module (EES25 or EES20) and from the used mode (Tx- or Fx- Mode)

Table 4-3 and 4-4 show port specification – Differential lines according to IEEE 802.3

Parameter (Tx-Mode, 10Base-T)		min.	typ.	Max.	Units
Output signal by 100 Ω		2,2		2,8	V
Input sensitivity switching on threshold				585	mV
Parameter (Tx-Mode, 100Base-Tx)		**min.**	**typ.**	**Max.**	**Units**
Output signal by 100 Ω		0,95		1,05	V
Symmetry output signal		98		102	%
Input sensitivity	switching on threshold switching off threshold	- 100		500 -	mV mV

Table 4-3: Electrical Specification Tx Mode

Parameter (Fx-Mode, 100Base-Fx)	min.	typ.	Max.	Units
Output signal by 100 Ω	0,5		2,4	V
Input sensitivity switching on threshold	500		2000	mV
Common Mode Range IFx Input	1,1		2,3	V
Output resistance		100		Ω
Input resistance		100		Ω

Table 4-4: Electrical Specification Fx Mode

Symbol	Description	min.	Typ.	Max.	Units
$f_{max\ SPI}$	Clock Frequency SPI		1	10	MHz
t_{su} (Setup time)	SPI_MOSI before SPI_Clk ↑	40			ns
	SPI_Clk ↑ before SPI_En1 ↑	40			ns

Symbol	Description	min.	Typ.	Max.	Units
	SPI_En2 before SPI_Clk ↑	40			ns
	SPI_MISO before SPI_Clk ↓	20			ns
	Parallel Data Input before SPI_En2 ↑	20			ns
t_h (Hold time)	SPI_MOSI after SPI_Clk ↑	20			ns
	SPI_MISO after SPI_Clk ↓	20			ns
	Parallel Data Input after SPI_En2 ↑	20			ns
t_{pd} (Output Delay)	SPI_MOSI after SPI_Clk ↑		0,5x $1/f_{max}$		ns
	SPI_MISO after SPI_Clk ↑	0		20	ns

Table 4-5: Timing Specification SPI

Parameter	min.	Typ.	Max.	Units
Operating PCB temperature (CASE) #1	-40		+90 #1	°C
Storage temperature	-40		+90	°C
Humidity (non-condensing)	10		95	%
Air-pressure by operating	795 (+2000 m a.s.l)			hPa
Air-pressure by storage	620 (+4000 m a.s.l)			hPa

Table 4-6: Miscellaneous

Note: The items marked with "#1" corresponds to temperature measurement point C1413 (see Fig. 4-1)

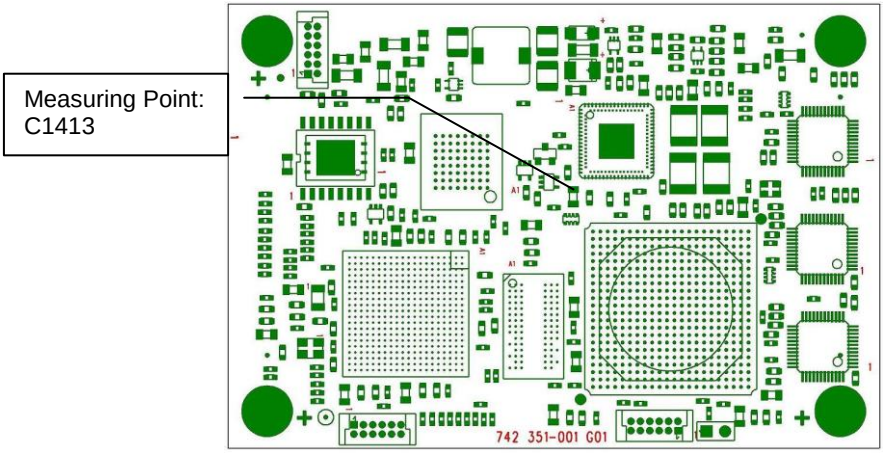


Figure 4-1: EES 25 and EES 20 – Temperature Measuring Point C1413

Name	Net weight	Units
EES25	80	g
EES20	70	g
Development Board	370	g

Table 4-7: Module Weights

4.1 Performance measured with development board

	Product Standard	Comment
Radiated Emission #1		
	EN 55022:2006+A1:2007 Class A, EN 55011:2007+A2:2007 Class A, EN 61131-2:2007, chapter 8.2.3 EN 61000-6-4:2007 EN 61850-3:2002, chapter 5.8 EN 50121-4:2006, chapter 1 and 5 FCC 47CFR:2009 Subpart B: Unintentional Radiators EN 61850-3:2002, chapter 5.8 Merchant Navy	
Conducted Emission #1		
Telecommunication Ports	EN 55022:2006+A1:2007 Class A EN 61000-6-4:2007	

Table 4-8: EMC Emission

Product Standard	Comment
Electrostatic Immunity #1	
EN61000-4-2 Test level equivalent to the requirements of EN 61000-6-2:2005 EN 61131-2:2007 EN 61850-3:2002 EN 50121-4:2006 IEEE 1613:2003 + A1:2008 Merchant Navy	8kV (Contact) 15kV (Air)
Electromagnetic Field #1	

Product Standard	Comment
EN61000-4-3 Test level equivalent to the requirements of EN 61000-6-2:2005 EN 61131-2:2007 EN 61850-3:2002 EN 50121-4:2006 IEEE 1613:2003 + A1:2008 Merchant Navy	20V/m
Burst #1	
EN61000-4-4 Test level equivalent to the requirements of EN 61000-6-2:2005 EN 61131-2:2007 EN 61850-3:2002 EN 50121-4:2006 IEEE 1613:2003 + A1:2008 Merchant Navy	4kV (Data lines)
Surge #1	
	4kV (Balanced Data lines)
Pulse magnetic field #1	
EN61000-4-4 Test level equivalent to the requirements of EN 50121-4:2006	300 A/m

Table 4-9: EMC Immunity Tests

Note: The items marked with "#1" were tested with Development Board

4.2 Physical performance

Product Standard	Comment
Operating Ambient Air Temperature #1	
IEC 60068-2-1, IEC 60068-2-2 Test level equivalent to the requirements of EN 61131-2:2007 EN 61850-3:2002 IEEE 1613:2003 + A1:2008 Merchant Navy	-40°C (16h) #3 85°C (16h) #3
Non Operating Ambient Air Temperature #1	
IEC 60068-2-1, IEC 60068-2-2 Test level equivalent to the requirements of EN 61131-2:2007 EN 61850-3:2002 IEEE 1613:2003 + A1:2008 Merchant Navy	-40°C (16h) #3 85°C (16h) #3
Damp Heat #1	
IEC60870-2-2, IEC 60068-2-30 Test level equivalent to the requirements of EN 61131-2:2007 EN 61850-3:2002 IEEE 1613:2003 + A1:2008 Merchant Navy	25°C /95% #3 55°C / 95% #3

Table 4-10: Climatic Tests

Note: The items marked with "#1" were tested with Development Board

Note: The items marked with "#3" were ambient air temperature

Product Standard	Comment
Vibration (Operating) #1	
IEC 60068-2-6 Test level equivalent to the requirements of EN 61131-2:2007 EN 61850-3:2002 IEEE 1613:2003 + A1:2008 Merchant Navy	2 Hz < f < 8,4 Hz 3,5mm 8,4 Hz < f < 200 Hz 1g 200 Hz < f < 500 Hz 1,5g sinusoidal vibration 1,0 g constant acceleration
Shock (Operating) #1	
IEC 60068-2-27 Test level equivalent to the requirements of EN 61131-2:2007 EN 61850-3:2002 IEEE 1613:2003 + A1:2008	15 g
MTBF Value	
EES 20	237,3 years GB 25 °C 89.7 years GB 60 °C
EES 25	205,9 years GB 25 °C 77,1 years GB 60 °C

Table 4-11: Mechanical Tests

Note: The items marked with "#1" were tested with Development Board

A Further Support

Technical Questions

For technical questions, please contact any Hirschmann dealer in your area or Hirschmann directly.
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